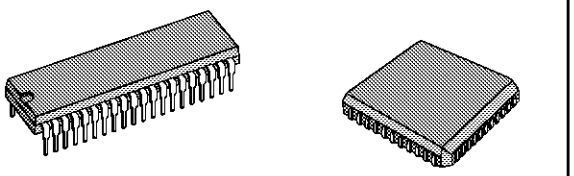
SGS-THOMSON MICROELECTRONICS

STLC5460

LINE CARD INTERFACE CONTROLLER

PRODUCT PREVIEW

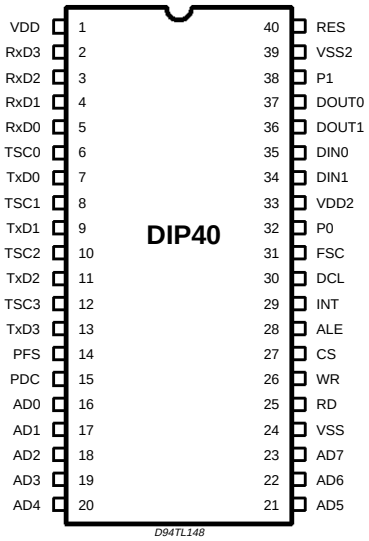
- BOARD CONTROLLER FOR UP TO 16 ISDN LINES OR 16 VOICE SUBSCRIBERS.
- TWO SERIAL INTERFACES :
  -PCM Four bidirectional multiplexes
  -GCI One (or two) at 2 Mb/s.
- NON BLOCKING SWITCH FOR 128 CHANNELS (16, 32 OR 64 KB/S BANDWIDTH).
- N CONSECUTIVE 64 kb/s CHANNELS FROM AN INPUT MULTIPLEX CAN BE SWITCHED AS A SINGLE N X 64 kbit/s CHANNEL TO AN OUTPUT MULTIPLEX AT 2048 kb/s.
- TIME SLOT ASSIGNMENT FREELY PROGRAMMABLE FOR EVERY CONNECTED SUBSCRIBER.
- PROGRAMMABLE PCM DATA RATES UP TO 8192 kb/s.CONSTANT DATA RATE AT 2 Mb/s ON GCI SIDE.
- PCM interface :
  - Simple and double clock frequency selectable;.
  - Programmable clock shift
  - Tristate mode control signals for extemal drivers.
- GCI interface :
  - Six bits or four bits Command/indicate channel selectable for analog or digital equipment
  - Command/Indicate Monitor channels validated or not
- Microprocessor access to two selected bidirectional channels of GCI and/or PCM.
- Multicontrollers for layer 1 functions :
  - C/I protocol controller for up to 16 C/I channels
  - Monitor protocol controller for up to 16 Monitor channels.
- Standard microprocessor interface with multiplexed address/data bus or separate address data buses.
- DIP40 PINS & PLCC44 pins PACKAGES

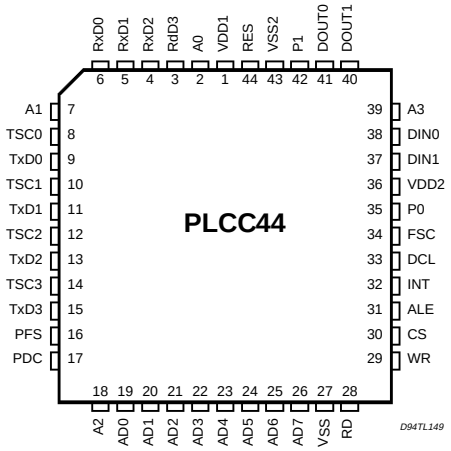


DIP40 **PLCC44**

ORDERING NUMBER: STLC5460

PIN CONNECTIONS (Top views)





DESCRIPTION

The Line Card Interface Controller, STLC5460, is a monolithic switching device for the path control of up to 128 channels of 16, 32, 64 kbps bandwidth. Two consecutive 64 kbps channels may also be handled as a quasi single 128 kbps channel. For these channels, the LCIC performs non-blocking space time switching between two serial interfaces, the system interface (or PCM interface) and the general component interface (GCI).

PCM interface can be programmed to operate at different data rates between 2048 and 8192 kbps. The PCM interface consists of up to four duplex ports with a tristate indication signal for each output line. The GCI interface can be selected to be PCM interface at 2Mbit/s.

The LCIC can be programmed to communicate with GCI compatible devices such as STLC3040 (SLIC), STLC5411 (U interface), ST5421 (S interface) and others. The device manages the layer 1 protocol buffering the Command/Indicate and Monitor channels for GCI compatible devices.

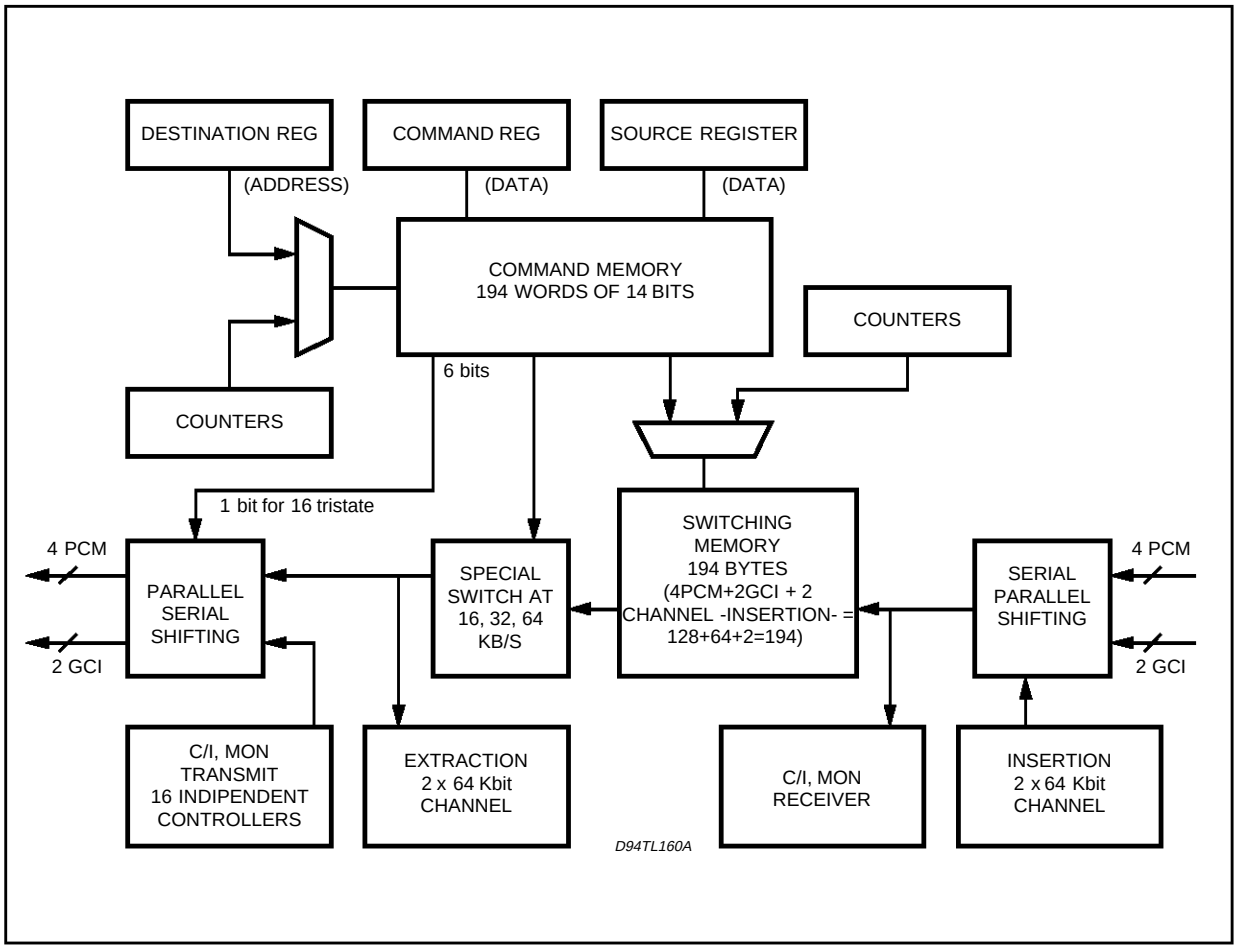
Due to its capability to switch channels of different bandwidths, the STLC5460 can handle up to 16 ISDN subscribers with their 2B+D channel structure in GCI configuration, or up to 16 analog subscribers. Since its interfaces can operate at different data rates, the LCIC is an ideal device for data rate adaption between PCM interface up to 8Mb/s and GCI at 2Mb/s.

Moreover, STLC5460 is one of the key building blocks for networks either with central, decentral or mixed signaling and packet data handling architectures associated with ST5451 (HDLC controller).

STLC5460 is available in a DIP40 or a PLCC44 package.

The DIP40 version is controlled by a standard 8 bit parallel microprocessor interface with a multiplexed address-data bus. In the PLCC 44 package, the device may optionally be controlled by separate address and data buses.

BLOCK DIAGRAM



PIN DEFINITIONS AND FUNCTIONS

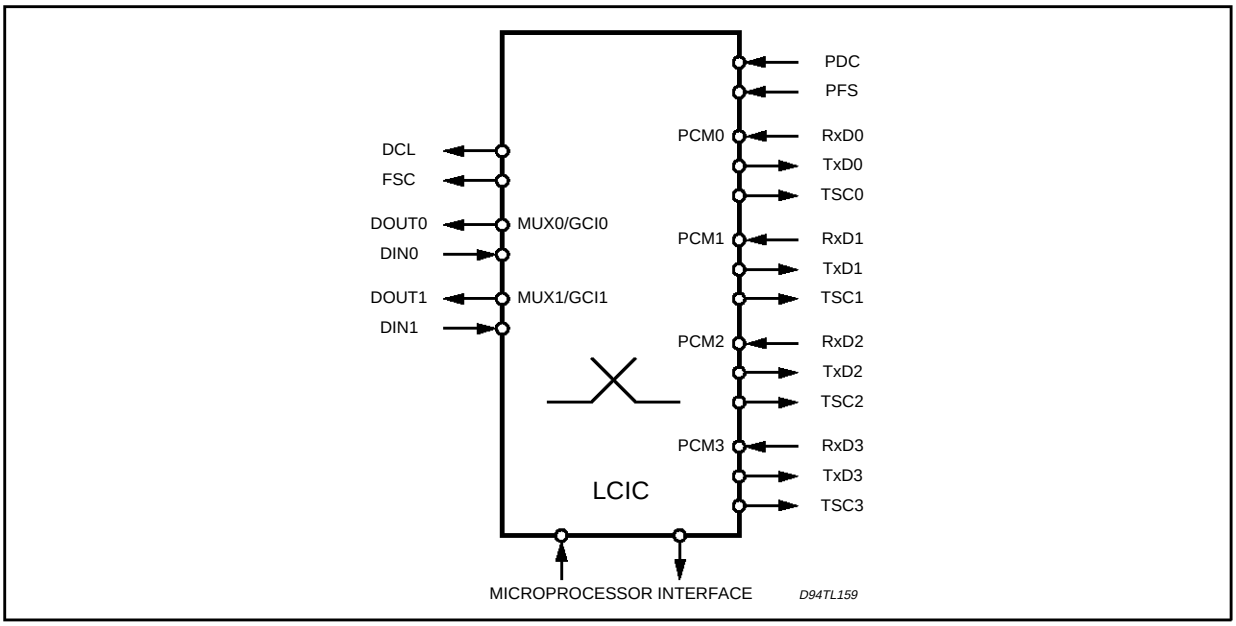
Symbol	Pin N DIP	Pin n PLCC	Type (*)	Function
VDD1	1	1	I	Supply Voltage 5V, ±5% .
A0	-	2	I	Address Bus Bit 0 : internal register address bus, bit 0.
RxD3 RxD2 RxD1 RxD0	2 3 4 5	3 4 5 6	I	Receive PCM interface Data : Serial data is received at these lines at standard TTL or CMOS levels.
A1	-	7	I	Address Bus Bit 1 : internal register address bus, bit 1.
TSC0 TSC1 TSC2 TSC3	6 8 10 12	8 10 12 14	OD	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
TxD0 TxD1 TxD2 TxD3	7 9 11 13	9 11 13 15	O	Transmit PCM interface Data : Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
PFS	14	16	I	PCM interface frame synchronization pulse.
PDC	15	17	I	PCM interface data clock, single or double rate.
A2	-	18	I	Address Bus Bit 2 : internal register address bus, bit 2.
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	16 17 18 19 20 21 22 23	19 20 21 22 23 24 25 26	I/O	Address Data Bus. If the multiplexed address/data P interface bus mode is selected these pins transfer data and commands between the P and the STLC5460. If a demultiplexed mode is used, these bits interface with the system data bus.
VSS1	24	27	I	Ground : 0V
RD	25	28	I	Read : The signal indicates a read operation, active low.
WR	26	29	I	Write : This signal indicates a write operatin, active low.
CS	27	30	I	Chip select. A low on this line selects the STLC5460 for a read/write operation.

(*): (I) Input
(O) Output
(IO) In/Output
(OD) Open Drain

PIN DEFINITIONS AND FUNCTIONS (continued)

Symbol	Pin N DIP	Pin n PLCC	Type	Function
ALE	28	31	I	Address latch enable. In the Intel type multiplexed P interface mode a logical high on this line indicates an address of a STLC5460 internal register on the external address/data bus. In the Intel type demultiplexed P interface mode, this line is hardwired to VSS, in the demultiplexed Motorola type P interface mode it should be connected to VDD.
INT	29	32	OD	Interrupt line, active low.
DCL	30	33	0	Data clock output.
FSC	31	34	O	Frame synchronization output.
PO	32	35	I	P0 associated to P1 selects the microprocessor interface (Motorola, Intel, ST9)
VDD2	33	36	I	Power supply : 5V
DIN1	34	37	I	GCI Data input 1
DIN0	35	38	I	GCI Data input 0
DOUT1	36	40	O	GCI Data Output 1
DOUT0	37	41	O	GCI Data Output 0
A3	-	39	I	Address Bus Bit 3 : Internal register address bus, bit 3..
P1	38	42	I	P1 associated to P selects the microprocessor interface (Motorola, Intel or ST9).
VSS2	39	43	I	Ground.
RES	40	44	I	Reset. A logical high on this input forces the STLC5460 into the reset state

Figure 1: GCI and PCM Interfaces.



LINE CARD APPLICATIONS

STLC5460 is designed both for digital and analog line card architectures.

It supports up to 16 ISDN subscribers or 16 voice subscribers. The level 1 devices are connected to ST5451 circuits to perform the D channel handling.

Analog Line Card

In analog line cards STLC5460 controls the signalling voice and data path of 64 kb/s channels.

In combination with STLC3040 and ST5451, it allows to perform an optimized line card architecture.

STLC5460 controls configuration of STLC3040 and transmits/receives signalling from the STLC3040.

Digital Line Card

In digital line cards STLC5460 controls configuration of Level 1 circuits (U or S Interface) by means MON channel configuration and performs activation/deactivation by means of Command/Indicate protocol. STLC5460 switches the B channels and can switch the D channels if the channel processing is centralized.

FUNCTIONNAL DESCRIPTION

PCM INTERFACE

The PCM Interface Registers configurate the data transmitted or received at the PCM port for:

- one PCM, the maximum data rate is 2048kb/s with four PCM ports (PCM Mode 0).
- one PCM, the maximum data rate is 4096kb/s with two PCM ports (PCM Mode 1).
- one PCM, the maximum data rate is 8192kb/s with one PCM port (PCM Mode 2).

The clock frequency of PDC is equal to or twice the data rate.

The rising edge of PFS signal is evaluated to determine the first bit of the first time slot of the frame. The length of PFS pulse is one bit-time at least and the length between two pulses is also one bit time.

After reset, STLC5460 is synchronized after two consecutive correct PFS pulses. Synchronization is lost by the device if the PFS signal is not repeated with the correct repetiton rate which has been stored by the circuit at the beginning of synchronization reserch.

LSYNC bit (interrupt register) at "1" indicates the synchronous state, a logical 0 shows that the synchronism has been lost.

Without programming the bit shift function of the PCM interface, the rising edge of the PFS signal marks the first bit of input and output PCM frame.

The Time Slot structure may be shifted using IPOF, OPOF and CPOF registers. The relation between the framing signal PFS and the bit stream is controlled by the contents of these registers. These registers denote the number of bit times, the PCM frame is shifted.

GCI INTERFACE

The Monitor Channel and the Command/Indicate channel may be validated or not. If not validated, the B3 and B4 channels become standard channels at 64 kb/s.

Command/Indicate channel if validated may be configurated with four bits for digital cards or six bits for analog cards.

The clocks (Bit clock and frame clock) are delivered by the device with double rate clocking or simple rate clocking

GCI		PCM			
Double clock DCL kHz	Data kb/s	PDC Clock (kHz)		Data rate kb/s	Mode
		Simple	Double		
4.096	2.048	2.048		2.048	Mode 0
4.096	2.048		4.096	2.048	Mode 0
4.096	2.048	4.096		4.096	Mode1
4.096	2.048		8.192	4.096	Mode 1
4.096	2.048	8.192		8.192	Mode 2
4.096	2.048		16.384	8.192	Mode 2

FSC and DCL are output signals derived from PFS and PDC which are input signals.

MEMORY STRUCTURE AND SWITCHING

The STLC5460 contains two memories, the Control Memory (CM) and Data Memory (DM).

Data Memory buffers the data input from the PCM interface and the data input from the GCI interface. Data Memory has a capacity of 128 + 64 time slots to buffer 4 PCM frame of 32 time slots and two GCI interfaces. It is written periodically once every 125µs controlled by the input counter associated to PCM interface and by the input counter associated to GCI interface. Data Memory is also used to perform the switching function and loopbacks.

The Control Memory has a capacity of 128 + 64 locations of 8 bits of control memory data and 6 bits of control memory code. The 14 bits are written via microprocessor interface and read cyclically under the control of the output counter associated to PCM interface and under the control of the output counter associated to GCI interface. The description of command register describes the different capabilities: switching at 64kb/s, 32kb/s, 16kb/s, loopback and also extraction/insertion from the microprocessor interface.

MICROPROCESSOR INTERFACE

The STLC5460 provides interface signals for Motorola type, Intel type and ST9 microprocessors. In the Intel type P interface mode either a multiplexed or a demultiplexed bus structure may be chosen.

For a demultiplexed bus structure the PLCC 44 package needs to be used, since only this package provides the additional lines of a separate 4 line address bus.

The ALE line of STLC5460 is used to control the bus structure and interface type. ALE is fixed to +5V for the Motorola type P interface and it is switching to signal an address or data transfer in the multiplexed Intel type P interface mode. Pins 28 and 29 of the PLCC package are interpreted as RD and WR for an Intel type interface or DS and R/W for a Motorola type interface.

For memory access, three registers are provided.

The destination register contains the address of a specific location of control memory; the source register contains the data (to be written or read) of the control memory. The control register contains the code (6 bits to be written or read) of the control memory.

A memory access using the actual command register and source register is performed upon every destination register write access. The processing of the memory access takes at most 488 ns.2.5.

EXTRA CHANNELS C/I AND MON CHANNELS

The Command/indicate and Monitor channels can be validated or not.

If validated, the C/I and MON protocol controllers operate and it is not possible to use this channels for switching.

If not validated, the protocols are inhibited and the channels can be used for switching.

COMMAND/INDICATE PROTOCOL

One configuration bit indicates the number of bits of the primitive (four or six bits) for all the channels. Eight (or sixteen) C/I channels are implemented.

To transmit a primitive into one of 16 channels, the primitive (4 or 6 bits) is loaded into source register and the C/I channel number is loaded into destination register with W/R bit of command register at "1".

With the same content in the destination register, the reading of the source register contains 4 (Or 6) last significant bits of the primitive which has not been transmitted yet, transmitted once, twice or more (two more significant bits).

To receive one primitive from sixteen channels, the process is the following :

An interrupt is generated when a new primitive has been received twice identical. Receive Number C/I Register contains the number of C/I channels (4 bits) and Auxiliary Memory contains the primitive received.

Moreover, the microprocessor can read directly the 16 primitives which have been received and stored into the Receive C/I Memory. To read this memory, Source Register contains the number of Receive C/I channel and destination register contains the primitive (4 or 6 bits) with a seventh bit which indicates whether the primitive has been received one or twice identical.

MONITOR CHANNEL PROTOCOL

Sixteen Monitor channels are implemented. To transmit message of one (or more) words, the first (and the next) is loaded into source register and the number of MON channels into destination register with W/R bit of Command Register at 1.

This byte is transmitted if BYTE Bit of Command Register is at 1.

To receive Message from sixteen Monitor channels, the process is the following : an interrupt is generated when a new byte has been received twice identical.

Receive Number Register contains the number of MON channels (4 bits) and receive data Monitor Channel Memory contains the last word received. The remote transmitter will transmit the next word after this register is read by the local microprocessor.

INSERTION - EXTRACTION

This capability allows to insert data to GCI interface and to PCM interface and to extract data from GCI interface and from PCM interface. This data is provided either by the microprocessor or by an internal Pseudo Random Sequence Generator.

INSERTION

Two programmable registers (Insert A and B) contain the data to insert into two outputs time slots continuously. To perform an insertion, four registers are programmed by the microprocessor.

- Insert A and/or B Registers for the data to insert.
- The Destination Register to indicate the output PCM or GCI interface and the number of Time Slot selected.
- If necessary, the Command Register to insert into 64 kb/s, 32 kb/s or 16 kb/s channel.

if two insertions are validated with two consecu-

tive time slots, a 128 kb/s channel is performed. When the data is inserted, status bit (INS) is put at logical 1. An interrupt is also generated.

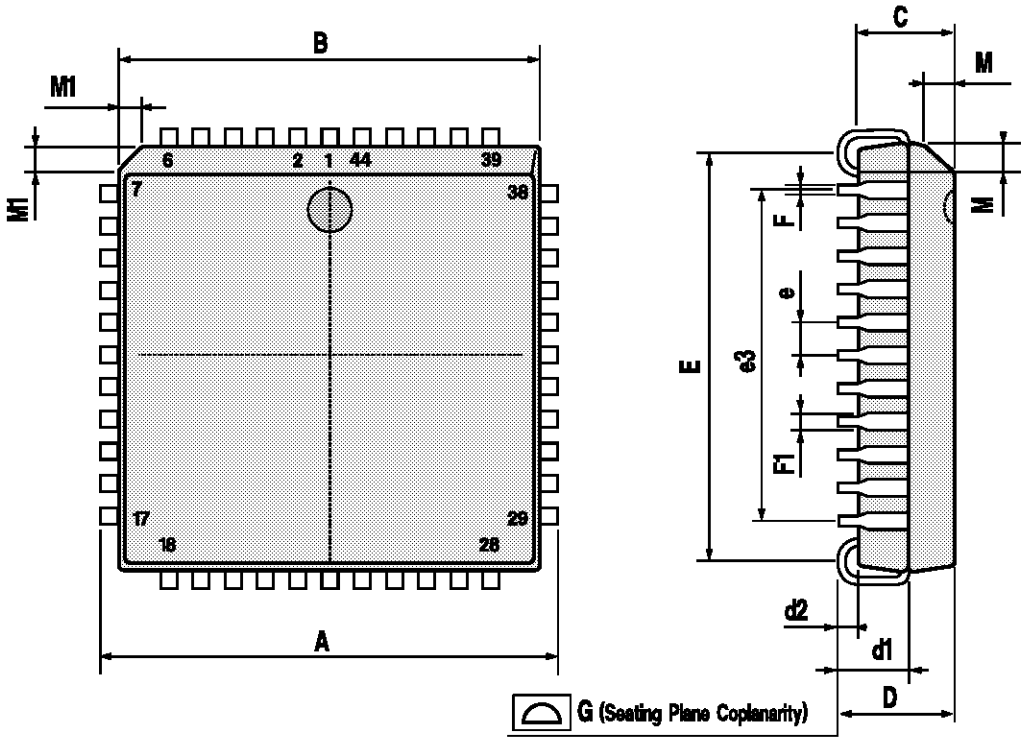
EXTRACTION

Two programmable registers (Extract A and B) contain the data extracted from two input time slots. To perform an extraction, three registers are programmed by the microprocessor :

- Extract A and/or B Registers for the data extracted.
- The Source register to indicate the input PCM or GCI interface and the number of Time Slot selected. if two insertions are validated with two consecutive time slots, data at 128 kb/s is extracted. When the data is loaded in Extract A or Extract B Register, Status Bit (EXT) is put at logical 1. An interrupt is also generated.

PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



DIP40 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130